REMARKS

The application has been reviewed in light of the final Office Action dated April 11, 2005 and the Advisory Action dated July 14, 2005. Claims 1, 2 and 10-15 were pending, with claims 1 and 10 being in independent form. Claims 3-9 were previously canceled, without prejudice or disclaimer. By this Amendment, new claim 16 has been added, and independent claims 1 and 10 have been amended to clarify the claimed invention. Accordingly, claims 1, 2 and 10-16 are now pending, with claims 1 and 10 being in independent form.

Claims 1, 2 and 10-15 were rejected under 35 U.S.C. §102(e) as purportedly anticipated by U.S. Patent No. 6,853,063 to Akiyama et al. Claims 1, 2 and 10-15 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,245,215 to Sawaya in view of U.S. Patent Application Publication No. 2003/0001808 A1 (Sakuma et al.).

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1 and 10 as amended are patentable over the cited art, for at least the following reasons.

This application relates to a semiconductor device responsive to different levels of input and output digital signals (for example, 5 volt high level signals and 3.3 volt high level signals). As is well known in the art, when a signal is said to have a "level" it is understood that the signal is a digital signal and the level of the digital signal refers to the driving voltage. Independent claims 1 and 10 have been amended to clarify this aspect of the claimed invention, although Applicant maintains that the claims would have been so understood by one skilled in the art even without the claim amendment.

Applicant devised a semiconductor device which integrates a plurality of semiconductor chips into a single package. A first semiconductor chip in the semiconductor device outputs one

or more first signals having a first level. A second semiconductor chip in the semiconductor device includes a signal level conversion circuit which converts the first signals from the first semiconductor chip into second signals having a second level different from (higher than) the first level. Thus, the first semiconductor chip can operate at lower voltage level, and the semiconductor device is nevertheless able to output signals at the second (higher) level which are acceptable to a device which operates at the second level. Each of independent claims 1 and 10 includes these features.

Akiyama, as understood by Applicant, is directed to a multi-chip type semiconductor device for a communication terminal. In the embodiment of Akiyama (column 8, line 1 through column 9, line 17) upon which the Office Action relies, the semiconductor device is applied to an analog front end (AFE) which includes an analog-to-digital circuit (ADC) and a digital-to-analog circuit (DAC). Although the Office Action fails to explicitly identify the correspondence between claim element and elements of Akiyama, the Office Action to the extent understood is believed to equate the ADC and DAC of Akiyama to the signal level conversion circuit. However, the ADC and DAC of Akiyama convert (i) an analog signal to a digital signal and (ii) a digital signal to an analog signal, respectively.

Applicant does not find disclosure or suggestion in Akiyama, however, of a semiconductor device which integrates a plurality of semiconductor chips into a single package, comprising a first semiconductor chip which outputs one or more first signals having a first level, and a second semiconductor chip which includes a signal level conversion circuit, wherein the signal level conversion circuit converts the first signals from the first semiconductor chip into second signals having a second level different from the first level of the first signals, and wherein the first level and the second level correspond to respective, different driving voltages in a digital

circuit, as provided by the claimed invention of independent claims 1 and 10.

Should the Examiner disagree therewith, Applicant requests that the Examiner cite to the specific column and line numbers in the cited reference where basis for the disagreement can be found.

Sawaya, as understood by Applicant, is directed to a multichip packaged semiconductor device. However, Sawaya is not directed at the problem that some chips operate at one level while other chips operate at a second level which is different from the first level.

As acknowledged in the Office Action, Sawaya does not find teach or suggest a signal level conversion circuit, wherein the signal level conversion circuit converts first signals having a first level into second signals having a second level different from the first level, as provided by the claimed invention of the present application.

Sakuma, as understood by Applicant, is directed to a liquid crystal display including a source driver comprising multiple source driver ICs. Each source driver IC includes a control circuit 21, an interface circuit 30, a shift register 22, a data latch 23, a D/A converter 24 and a buffer amplifier 25. The D/A converter 24 converts a digital gamma correction signal to an analog signal and outputs the analog signal to the buffer amplifier 25.

However, the D/A converter 24 and buffer amplifier 25 of Sakuma does not disclose or suggest a signal level conversion circuit which converts first signals from a first semiconductor chip into second signals having a second level different from the first level of the first signals, wherein the first level and the second level correspond to respective, different driving voltages in a digital circuit, as provided by the claimed invention of independent claims 1 and 10.

Applicant simply does not find disclosure or suggestion in the cited art of a semiconductor device which integrates a plurality of semiconductor chips into a single package,

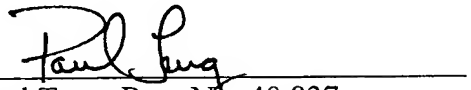
comprising a first semiconductor chip which outputs one or more first signals having a first level, and a second semiconductor chip which includes a signal level conversion circuit, wherein the signal level conversion circuit converts the first signals from the first semiconductor chip into second signals having a second level different from the first level of the first signals, and wherein first level and the second level correspond to respective, different driving voltages in a digital circuit, as provided by the claimed invention of independent claims 1 and 10.

In view of the claim amendments and remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,



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